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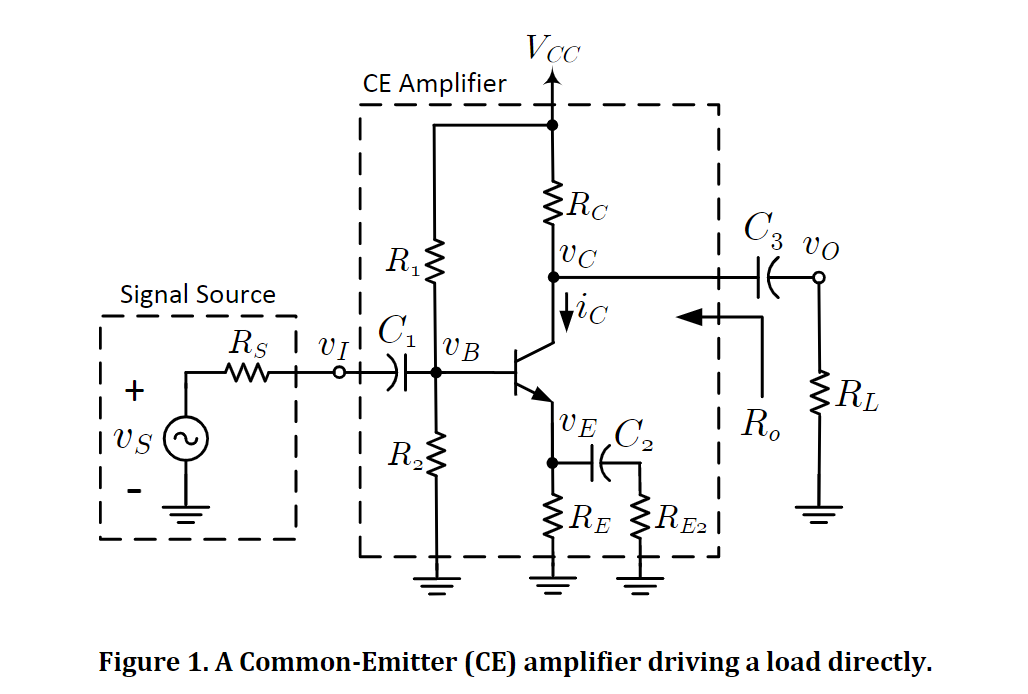
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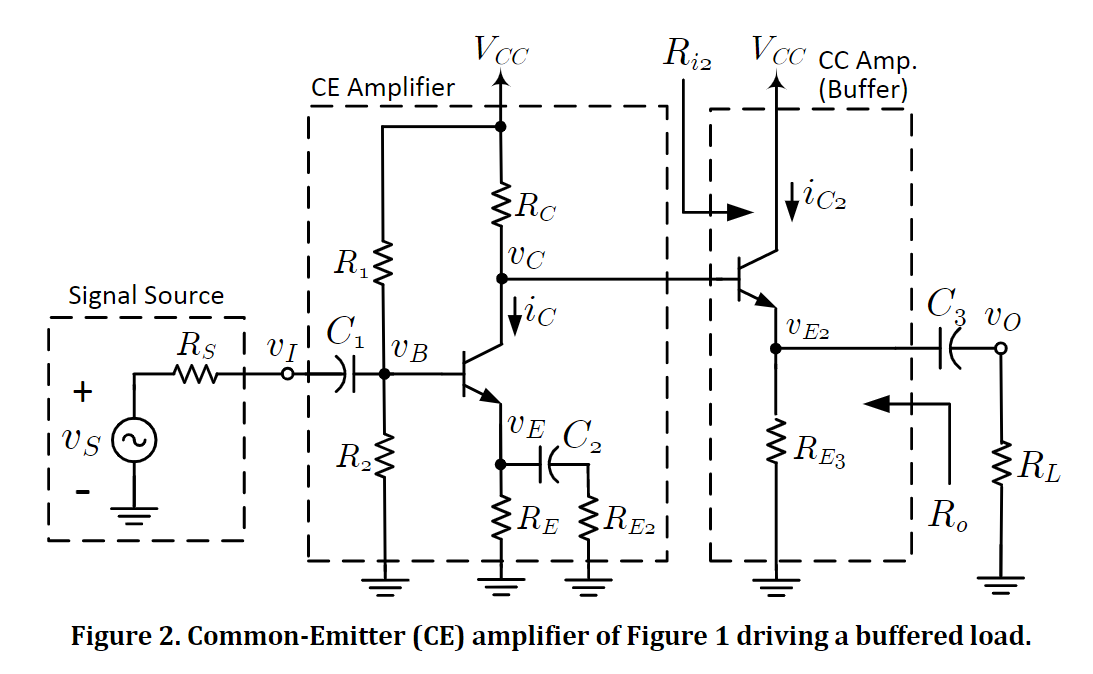
**Introduction and Objectives**

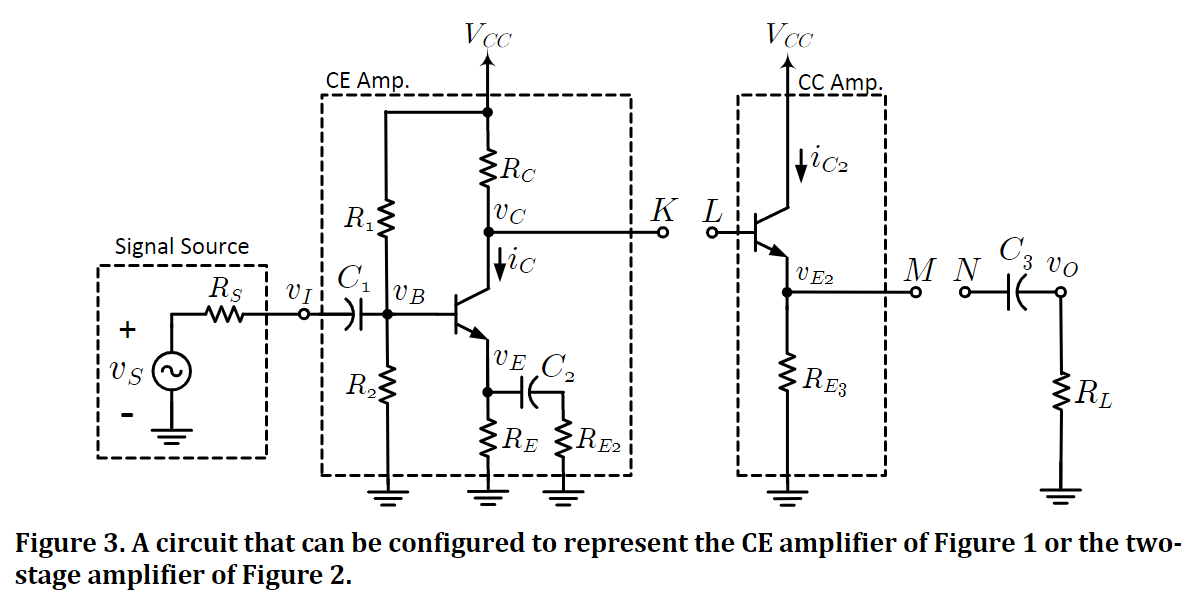
In this lab, we will be creating a common-collector BJT amplifier. The objective of this lab is to test and learn more in-depth about buffering and its use in the amplifier circuits. After a simple CE amplifier, it will then be evolved into a two-stage amplifier (CC) and then tested once again.

**Experimental Results**

**Figure 1** below is the CE portion of out two-stage amplifier that will be implement later, in **Figure 2,** and tested as **Figure 3,** which can be modified to be either **Figure 2** or **Figure 1.**







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**Figure 3(a).** Circuit created based on schematic from **Figure 3,** without any jumpers attached.

E1.

The power supply was set as close as possible to 15V, and the circuit of **Figure 3(a)** was created. Next, using the multimeter, the required values in **Table E1** below were measured and recorded, and the currents were calculated, with either no jumpers, or with the K-L jumpers attached, transforming the circuit into a two-stage amplifier.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Amplifier | Jumpers | Vc [V] | Ve [V] | Ic [mA] | Ve2 [V] | Ic2 [mA] |
| CE  (Figure 1) | None | 10.8 | 7.88 | 0.23 | ----- | ----- |
| Two-stage  (Figure 2) | K-L | 10.58 | 7.88 | 0.19 | 10.35 | 0.44 |

**Table E1.** Quiescent parameters of CE amp. of **Figure 1** and two-stage amp. of **Figure 2.**

E2.

Next, jumpers were removed, putting the circuit back to its state in **Figure 3.** The signal generator was then attached to the circuit. At our station, our values from **Table E1** were tested and deemed correct by the TA, and the circuit was checked and proven to be correct as well, however, out station appeared to have faulty equipment of sorts, meaning our oscilloscope could not get correct readings, and the values we have used from this point on, have been collaborated on with another group, as verbal instructions from the TA have stated during the lab session. However, the circuit was redesigned and simulated in multisim in order to have a correct graph shown. **Table E2(a)** values were measured, and the rest of the values were calculated from those values.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Amplifier | Jumpers | vi [Vrms] | vc [Vrms] | ve2 [Vrms] | vo [Vrms] | Avo [V/V] |
| CE | None | 66.23 mV | 0.712 V | --- | --- | 10.75 |

**Table E2(a).** No-load AC voltages and gain of the CE amplifier of **Figure 1.**

Next, the K-N jumper was put back into the circuit, and the values were measured once again.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Amplifier | Jumpers | vi [Vrms] | vc [Vrms] | ve2 [Vrms] | vo [Vrms] | Avo [V/V] |
| CE | K-N | 66 mV | 0.652 | --- | 0.637 | 9.65 |

**Table E2(b).** Loaded AC voltages and gain of the CE amplifier of **Figure 1.**

E3.

The K-N jumper was removed and was replaced with the K-L jumper. This circuit is now a two-stage, no load amplifier. From here, the values of **Table E3(a)** were measured and recorded.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Amplifier | Jumpers | vi [Vrms] | vc [Vrms] | ve2 [Vrms] | vo [Vrms] | Avo [V/V] |
| Two-stage | K-L | 66 mV | 0.7 | 0.7 | --- | 10.6 |

**Table E3(a).** No-load AC voltages and gain of the two-stage amplifier of **Figure 2.**

Now, the M-N jumper was attached, and the measurements were taken once again. The waveform is shown below, and the measured values are also listed in the table below.

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**Graph E3.** Waveform of Vo and Vi, of the two-stage amplifier, with K-L and M-N jumpers connected.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Amplifier | Jumpers | vi [Vrms] | vc [Vrms] | ve2 [Vrms] | vo [Vrms] | Avo [V/V] |
| Two-stage | K-L, M-N | 66 mV | 0.65 | 0.637 | 0.63 | 9.6 |

**Table E3(b).** Loaded AC voltages and gain of the two-stage amplifier of **Figure 2.**

**Conclusions and Remarks**

C1.

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**Equation 1.** Equation used to calculate percentage error.

Calculations of the error percentages (for C1 and C2):

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|  |  |  |  |
| --- | --- | --- | --- |
|  | Vc [V] | Ve [V] | Ve2 [V] |
| Calculated values  (From Table P1) | 11.98 | 7.63 | ----- |
| Measured values  (First row, Table E1) | 10.8 | 7.88 | ----- |
| Percent error, e% | 10.9% | 3.17% | ----- |

**Table C1(a).** Calculated and measured (DC) voltages of the CE amplifier of **Figure 1.**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Vc [V] | Ve [V] | Ve2 [V] |
| Calculated values  (From Table P2) | 12.0 | 7.58 | 9.44 |
| Measured values  (Second row, Table E1) | 10.58 | 7.88 | 10.35 |
| Percent error, e% | 13.4% | 3.81% | 8.79% |

**Table C1(b).** Calculated and measured (DC) voltages of the two-stage amplifier of **Figure 2.**

Some possible sources of error are the power supply not being exactly 15V, as it was in the manual calculations. Other potential reasons for discrepancies are the fact that experimentally, our resistors, wires and transistors are not ideal. Further, our Rbe might not be 0.7 exactly, as we assumed in the calculations.

C2.

|  |  |  |
| --- | --- | --- |
|  | Av [V/V] | Avo [V/V] |
| Calculated Values  (From Table P1) | 7.1 | 7.03 |
| Measured Values  (From Table E2(a) and Table E2(b)) | 10.75 | 9.65 |
| Percent error, e% | 34% | 27.2% |

**Table C2(a).** Calculated and measured voltage gains of the CE amplifier of **Figure 1.**

|  |  |  |
| --- | --- | --- |
|  | Av [V/V] | Avo [V/V] |
| Calculated Values  (From Table P2) | 5.62 | 5.39 |
| Measured Values  (From Table E3(a) and Table E3(b)) | 10.6 | 9.6 |
| Percent error, e% | 47% | 43.9% |

**Table C2(b).** Calculated and measured voltage gains of the two-stage amplifier of **Figure 2.**

Some possible sources of error are the power supply not being exactly 15V, as it was in the manual calculations, or that our signal generator was not exactly 1kHz. Other potential reasons for discrepancies are the fact that experimentally, our resistors, wires and transistors are not ideal. Further, our Rbe might not be 0.7 exactly, as we assumed in the calculations, and the wires would have some resistance, which is not accounted for in the calculated portion.

C3.

If Rout >> RL, most of the voltage drop occurs at Rout, so little drops at RL, and this is the loading effect. In this case, the output impedance of the CE circuit matches the input impedance of the CC circuit. CE output impedance is RC, and input impedance of CC is (β+1)(re + Re3 || RL). So, RL > Rout. Rout of CC is ~ Re3(RC/ β+1). CC is a buffer, so the gain will be ~1. This is far superior.

**Appendix**

Submitted TA copy of results.

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Submitted Pre-lab 7.

Diagram

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Description automatically generated Text, letter

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NOTE: Small error on graph P2: Ie2 [mA] should be Ve2 [V]!

Graphical user interface, chart

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